COMPLETE SET OF PENDING CLAIMS

What is claimed is:

1. (Currently Amended) A chip-scale package comprising:

a substrate having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;

a memory die having a first surface and an opposite second surface, the first surface of the memory die mounted ~~on~~ facing the first surface of the substrate, the memory die is electrically coupled to the substrate using a plurality of rigid underside coupling members, the substrate having a coefficient of expansion that ~~substantially~~ matches a coefficient of expansion of the memory die to within six parts per million per degree Celsius or less, wherein the second surface of the memory die remains completely exposed;

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration adjacent to the memory die, at least one of the solder balls electrically coupled to at least one of the underside coupling members;

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme; and

one or more electronic components mounted on the second surface of the substrate in an area substantially opposite of the memory die, wherein the combined distance that an electronic component and the memory die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

2. (Currently Amended) The chip-scale package of claim 1 further comprising:

electrically conductive traces on the first surface to electrically couple at least one solder ball to the memory die directly.

3. (Currently Amended) The chip-scale package of claim 1 wherein ~~the substrate includes a controlled thermal expansion material that sufficiently matches the coefficient of expansion of~~

~~the memory die.~~ the plurality of rigid underside coupling members are a second plurality of solder balls.

4. (Currently Amended) The chip-scale package of claim 1 wherein ~~the underside coupling members permit the underside surface of the memory die to be substantially exposed.~~ five sides of the memory die are completely exposed and the first surface of the memory device is substantially exposed for improved heat dissipation.

5. (Currently Amended) A chip-scale package comprising:

a substrate having a first surface and an opposite second surface;

a semiconductor device mounted on the first surface of the substrate using a plurality of electrical conductors ~~solder balls~~, the semiconductor device having a first surface and an opposite second surface, the first surface of the semiconductor device mounted facing the first surface of the substrate, wherein the second surface of the memory die remains completely exposed for improved ventilation;

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration adjacent to the semiconductor device, at least one of the solder balls electrically coupled to the semiconductor device; and

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing scheme which, when a plurality of chip-scale packages is stacked together, causes a solder ball of a first chip-scale package to be uniquely electrically coupled with an electrical conductor of a semiconductor device mounted on a second chip-scale package N levels from the first chip-scale package, where N is an integer greater than two.~~; and~~

~~one or more electrical components mounted on the second surface of the substrate~~.

6. (Currently Amended) The chip-scale package of claim 5~~wherein the~~ further comprising: one or more electrical components ~~are~~ mounted on the second surface of the substrate in an area substantially opposite of the semiconductor device.

7. (Cancelled)

8. (Currently Amended) The chip-scale package of claim ~~5~~ 6 wherein the combined distance that ~~an~~ one or more electrical ~~component~~ components and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

9. (Currently Amended) The chip-scale package of claim 5 wherein the substrate includes a controlled thermal expansion material with a coefficient of expansion that substantially matches the coefficient of expansion of the semiconductor device to within six parts per million per degree Celsius or less.

10. (Cancelled)

11. (Currently Amended) The chip-scale package of claim 5 further comprising:

electrically conductive traces on the first surface to ~~electrically~~ directly couple at least one solder ball to the semiconductor device.

12. (Original) The chip-scale package of claim 5 wherein the semiconductor device is a silicon memory device.

13. (Cancelled)

14. (Cancelled)

15. (Currently Amended) A stackable electronic assembly comprising:

a plurality of chip-scale packages, the plurality of chip-scale packages arranged in a stacked configuration, each chip-scale package including

a substrate having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;

a semiconductor device coupled to traces on the first surface of the substrate using underside coupling members~~, the substrate having a coefficient of expansion that substantially matches a coefficient of expansion of the semiconductor device~~;

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration adjacent to the semiconductor device, at least one of the solder balls electrically coupled to the semiconductor device; and

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a staggered routing ~~scheme; and~~ scheme,

~~one or more electrical components mounted on the second surface of the substrate in an area substantially opposite of the semiconductor device, wherein the combined distance that an electronic component and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate;~~

wherein all chip-scale packages in the stacked configuration have identical routing traces.

16. (Currently Amended) ~~A~~ The stackable electronic assembly of claim 15 wherein ~~the plurality of chip-scale packages have identical routing traces~~ the substrate having a coefficient of expansion that substantially matches a coefficient of expansion of the semiconductor device to within six parts per million per degree Celsius or less.

17. (Currently Amended) ~~A~~ The stackable electronic assembly of claim 15 wherein the solder balls on the first surface of a first chip-scale package are coupled to the pads on the second surface of a second chip-scale package.

18. (Currently Amended) ~~A~~ The stackable electronic assembly of claim 15 ~~wherein the staggered routing scheme permits accessing the same underside coupling member in each of the chip-scale packages in a stack from a plurality of solder balls in a first chip-scale package.~~ wherein the staggered routing scheme causes a solder ball of a first chip-scale package of a stack configuration to be uniquely electrically coupled with an underside coupling member of a semiconductor device mounted on a second chip-scale package N levels from the first chip-scale package, where N is an integer greater than two.

19. (Currently Amended) The stackable electronic assembly of claim ~~15~~ 18 wherein ~~the underside coupling members permit the underside surface of the semiconductor device to be exposed.~~ the staggered routing scheme is stepped as it moves up the plurality of chip-scaled packages of a stacked configuration.

20. (Currently Amended) A memory module comprising:

a main substrate with an interface to couple the memory module to other devices; and

one or more stacks of memory devices coupled to a first surface of the main substrate,

at least one stack of memory devices including

a plurality chip-scale packages, the plurality of chip-scale packages arranged in a stack ~~stacked configuration~~, all chip-scale packages in the stack ~~and~~ having identical routing traces ~~on a first surface and opposite second surface of the chip-scale package~~ at every level of the stack, each chip-scale package including

a substrate having a first surface and an opposite second surface,

a memory semiconductor die electrically coupled to traces on the first surface of the substrate ~~using underside coupling members~~, and

a plurality of solder balls mounted on the first surface of the substrate adjacent to the memory semiconductor die, at least one of the solder balls electrically coupled to the memory semiconductor die.

21. (Currently Amended) The memory module of claim 20 wherein

the substrate is composed of a controlled thermal expansion material,

the substrate has a coefficient of expansion that substantially matches a coefficient of expansion of the memory semiconductor die to within six parts per million per degree Celsius or less,

wherein five sides of the memory semiconductor die are completely exposed and a sixth side of the memory semiconductor die is substantially exposed for improved heat dissipation, and

~~the plurality of solder balls are mounted on the first surface of the substrate in a ball grid array configuration, and~~

each chip-scale package further includes

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a stepped staggered routing scheme, and

one or more electronic components mounted on the second surface of the substrate in an area substantially opposite of the memory semiconductor die, wherein the combined distance that an electronic component and the memory semiconductor die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

22. (Currently Amended) The memory module of claim 21 wherein ~~the staggered routing scheme permits accessing the same underside coupling members in all of the chip-scale packages in a stack from a plurality of solder balls in a first chip-scale package~~ the staggered routing scheme forms an electrical path from a first chip-scale package of a first stack that moves inward toward the memory semiconductor die mounted on a second chip-scale package N levels from the first chip-scale package, where N is an integer greater than two, as the electrical path moves up through each layer of the first stack.

23. (Original) The memory module of claim 20 wherein the memory module is a dual inline memory module.

24. (Original) The memory module of claim 20 further comprising:

one or more stacks of memory devices coupled to a second surface of the main substrate.

25. (Cancelled)

26. (Cancelled)

27. (New) A stackable electronic assembly of claim 15 wherein the coefficient of expansion of the controlled thermal expansion material substantially matches the coefficient of expansion of the semiconductor device to within six parts per million per degree Celsius or less.

28. (New) The stackable electronic assembly of claim 15, the semiconductor device having a first surface and an opposite second surface, the first surface of the semiconductor device mounted towards the first surface of the substrate, wherein the second surface of the memory die remains completely exposed for improved ventilation.

29. (New) The stackable electronic assembly of claim 28 wherein five sides of the semiconductor device are completely exposed and the first surface of the memory device is substantially exposed for improved heat dissipation.

30. (New) The stackable electronic assembly of claim 15 further comprising:

one or more electrical components mounted on the second surface of the substrate in an area substantially opposite of the semiconductor device, wherein the combined distance that an electronic component and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

31. (New) The stackable electronic assembly of claim 19 wherein the staggered routing scheme forms an electrical path from a first chip-scale package of a stacked configuration that moves inward toward the semiconductor device mounted on a second chip-scale package N levels from the first chip-scale package, where N is an integer greater than two, as the electrical path moves up through each layer of the stacked configuration.

32. (New) The stackable electronic assembly of claim 31 wherein the electrical path moves from the first chip-scale package of a stacked configuration to a last chip-scale package of the stacked configuration along one side of the stacked configuration.